

Sam A. Mahmoud
3725 Adriatic Way
Santa Clara, California 95051
phone: 408-260-9560
email: "ee" underscore "sam" at "sammahmoud.com"

Professional Objective: A leadership role in ASIC design, verification, or applications.

Summary of Strengths:

Fifteen years experience in ASIC design and applications. Expert in architecture definition, RTL coding, logic verification, synthesis, simulation, static-timing analysis, evaluating EDA tools, and developing CAD flows. Experience in customer support, lab debug/bringup, and circuit board design. MSEE from a top-10 ranked graduate school. Articulate in person and in writing; commended on presentation skills.

Employment:

10/2003 present: Sr. Applications Consultant, Synopsys, Mountain View, CA

The sole west-coast applications specialist in Formality, Synopsys' equivalence checking tool. Coordinated account activity for entire North America West region. Responsible for all technical pre-sales support related to this tool, from giving initial presentations through ensuring technical success in customer evaluation benchmarks. Taught seminars, lunch-and-learn sessions, and training classes. Performed direct customer support at key accounts to ensure success with, and increase usage of, the tool. Trained other applications consultants to support the tool. Often consulted by R&D to help define and prioritize feature improvements.

2002-2003: Digital Design Manager, Nexio Systems, Scotts Valley, CA

As the sole digital design expert in a new PCI-Express startup, built entire digital design infrastructure from scratch while also doing hands-on design work. Developed and documented a micro-architecture for a PCI-Express to PCI-X bridge. Evaluated scheduling algorithms for a crossbar switch. Analyzed feasibility (gate-count, power, schedule, and performance) of the company's chip and modified the architecture accordingly. Evaluated and selected EDA tools (a Verilog simulator and synthesis tools). Evaluated and selected a PCI-X core. Prepared company's plan for integration of analog and digital design flows for integration of Phy/SERDES with digital. Created company standards for Verilog coding style and source control. Interviewed engineers and made hiring decisions. Made outsourcing decisions. Prepared materials for presentations to venture capitalists. Analyzed market predictions and made revenue projections. Wrote a company white paper.

2000-2002: Staff Design Engineer, Cypress Semiconductor/HiBand Semiconductor

Responsible for digital functionality and chip-level integration of a quad 2.5Gbps and 3.125Gbps Phy (SERDES) for 10G Ethernet. Responsible for design flow from front to back: Verilog RTL design, synthesis, verification, test vector generation, creating

CAD flows, assembly/packaging drawings, interfacing with test and product engineering, lab debug/bringup and characterization, training the FAE organization about our product, and some direct customer support. Led the effort to get the group's first design through Cypress' design review processes. Worked on methods for mixed analog-digital verification. Wrote a power analysis utility, producing the company's best pre-tapeout power analysis and eliminating the need to buy an EDA tool.

1998-2000: Senior Design Engineer: Silicon Spice, Mountain View, CA

As a key member of a small design team that built an 80-million-transistor system-on-a-chip in 0.18 micron, architected and implemented a subsystem of four different I/O ports and their complex data paths into main memory. Owned this subsystem from start to finish: created the requirements, wrote the microarchitecture specifications, wrote the Verilog RTL, and completed verification, synthesis, and timing closure. These I/O ports communicated with four different bus protocols, and included several complex DMA engines. Proactively determined the needs of such diverse groups as CAD team, EDA vendors, test engineers, DFT engineer, marketing, and systems team to create an efficient, robust, re-usable design. Demonstrated leadership by stepping forward to solve group-wide problems: worked on coding style standard, evaluated and selected EDA tools for the team (a Verilog simulator, a lint tool, and a formal verification tool), took the first design through the new design review process and the first design blocks through the new synthesis process, and introduced the first lint and formal verification practices in the company.

1995-1998: Senior Design Engineer: GEC Plessey Semiconductors, San Jose, CA

Customer support engineer (FAE) for a CMOS ASIC vendor. Used a diverse mix of skills to address issues spanning all aspects of the business to ensure the ultimate success of customers' ASIC design projects. Management responsibilities included: scheduling projects, training staff, mentoring new engineers, recommending hardware and software purchases, interviewing engineers, specifying company's new product capabilities, supervising layout work, and assessing the feasibility and cost of proposed new ASIC projects. Technical responsibilities included: digital design in Verilog, synthesis, simulation, verification, test vector generation and manipulation, CAD support, inventing and proving new design methodologies, performing turn-key FPGA-to-ASIC conversions, and creating continuous improvement of CAD flows. People-oriented responsibilities included: customer visits with sales and marketing, acting as a source of design guidance and expertise to customer design engineers, traveling internationally to present on technical topics, and acting as the first line interface to customers and to the factory.

1994-1995: Senior ASIC Designer: Stac Electronics, Carlsbad, CA

Solely responsible for defining the requirements, specifications, and architecture for a next generation data compression chip. In parallel, evaluated and selected a suite of CAD tools and created a design flow to be used for all future ASIC designs.

1993-1994: Development Engineer: Teradyne, Agoura Hills, CA

Designed a 200MHz ECL/GaAs gate array (50K gates plus embedded RAM) to be the instruction processor for a special-purpose computer. Solely responsible for all phases from digital design through simulation/verification, refinement, and release to vendor, including 100% fault coverage and strategies for meeting extremely difficult timing requirements. Independently responsible for meeting project schedule.

1992-1993: Senior Engineer - Electrical: Harris Corp, Melbourne, FL

Developed a PCB and a multi-chip module for a fiber-optic LAN for the F-22 fighter aircraft. Responsibilities included crosstalk isolation, decoupling, meeting difficult mechanical constraints, addressing reliability and manufacturability concerns. Duties included interfacing with a partner firm and making presentations to the customer.

1990-1992: Associate Design Engineer: NCR Corp (National Cash Register), Liberty, SC

Designed motherboards for high performance PCs with custom architectures. Solely responsible for creating the largest circuit board that had ever been made by the plant, a motherboard for NCR's flagship server product that was proclaimed "The World's Fastest PC" and was featured on the cover of Personal Workstation magazine. Responsible for all phases of motherboard development: digital design, board-level debug, manufacturability, layout, and functional specification.

Summer 1989: Engineer Intern, Honeywell, Minneapolis, MN

Worked as part of a design team developing a new furnace control product. Also worked independently to modify and miniaturize an existing hot-tub controller.

Education:

1988-1989: Georgia Institute of Technology (Georgia Tech), Atlanta, GA

Master of Science in Electrical Engineering, December 1989; concentrations in computer engineering and control systems. Graduate education financed by research assistantship in Computer Integrated Manufacturing Systems and a teaching assistantship.

1986-1988: University of New Orleans, New Orleans, LA

Bachelor of Science in Electrical Engineering with Honors in Electrical Engineering, May, 1988. Education partially financed by working in a research laboratory. Submitted and orally defended an honors thesis.

Other Skills:

Experienced with a wide variety of CAD/EDA tools, and expert in evaluating them and making them work together. Skilled at defining microarchitecture and functional specifications. Able to program in Perl, TCL, C, Awk, Fortran, Pascal, and Unix shell scripts. Experience with large system-on-a-chip projects, including the integration of embedded IP cores. Experience with circuit-board design and manufacturing, and hands-on lab work. Experience with customer support and applications engineering. Able to create detailed requirements specs and design methodologies from scratch.

Registration: Registered Professional Engineer(PE), State of California. Member, IEEE.

Keywords:

ASIC design, architecture, microarchitecture, Verilog, Cadence, Synopsys, Design Compiler, Ambit, BuildGates, simulation, synthesis, verification, logic, digital design, FPGA, VCS, Design For Testability, Unix, C, Perl, TCL, Exemplar, Leonardo, Galileo, CAD, CAE, EDA, applications, FAE, SoC, system on a chip, formal verification, verilint, chrysalis, Formality.

Personal: Citizenship: U.S.A
 Date of Birth: February 19, 1967